## REMARKS

Claims 1-25 were pending in the application prior to this action.

The Examiner objects to claim 18 as being dependent on a rejected base claim but would be allowable if rewritten in independent form to include the limitations of the base and any intervening claims. The Examiner rejects claims 1-4, 9-12, 15, and 17 under 35 U.S.C. § 102(e) as being anticipated by Kim (U.S. Pat. No. 6,219,023 B1). The Examiner rejects claims 5, 13, 16, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Choi et al (U.S. 5,742,349). The Examiner rejects claims 6-8, 14, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Faroudja et al (U.S. 6,222,589). The Examiner rejects claims 20-21 and 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Imaizumi et al (U.S. 2002/0158868).

The applicants amend claims 1-4, 7-11, 15, and 17-18.

The application remains with claims 1-25.

The applicants add no new matter and request reconsideration.

### Claim Objection

The applicants rewrite claim 18 in independent form to include all the limitations of base claim 15 and intervening claim 17.

Claim 18 is in condition for allowance.

### Claim Rejections under 35 U.S.C. § 102(e)

Claim 1 recites *a failsafe circuit to generate an internal vertical refresh rate...being a predetermined fraction of the input vertical refresh rate.* Claim 9 recites *a failsafe circuit to generate an internal vertical refresh rate a predetermined fraction of the input vertical refresh rate....* Claim 15 recites *the internal vertical refresh rate being a factor of the input vertical refresh rate.* Claim 19 recites *generating an internal vertical refresh rate... being a predetermined factor of the input vertical refresh rate.* In each case, the failsafe circuit generates an internal vertical refresh rate that is different (e.g., a factor different than the input vertical refresh rate) than the input vertical refresh rate.

Notwithstanding the Examiner's allegations, Kim does not disclose changing the vertical refresh rate under certain conditions much less generating an internal vertical refresh rate that is a fraction of the input vertical refresh rate responsive to a failsafe enable signal.

Kim discloses at column 4, lines 59-61:

"With the apparatus, the frequency of the vertical synchronization signal Vsync is kept constant..."

Kim discloses at column 5, lines 24-30:

"Next, if the SVGA mode signals are fed to the LCD controller (i.e., the video signal converter) according to this embodiment, the frequency of the vertical synchronization signal Vsync is kept constant..."

Table 1 discloses a system in which the vertical refresh signal Vsync is kept constant while the horizontal refresh signal Hsync and the dot clock Dclk are increased relative to the input frequency. Again, the vertical refresh signal does not change.

We can only conclude that the Examiner misunderstood the invention recited in the claims. Claims 1-25 are novel and not obvious over Kim and any other reference cited by the Examiner. Claims 1-25 are in condition for allowance.

**Conclusion**

The applicants request reconsideration and allowance of all claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613
**Customer No. 20575**

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on May 11, 2004.

Beth Nichols